CLAIMS

1. A method of activating a display element of a display device having n x m array of display elements, each display element coupled to a logic controlled switch, the method comprising:

applying a row address input and a row electrode input to control logic of the logic controlled switch of the display element;

applying a column address input and a column electrode input to the control logic of the logic controlled switch of the display element;

activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

15

10

5

2. The method of Claim 1,

comparing the row address input and the row electrode input, comparing the column address input and the column electrode

20

input,

activating the display pixel with the logic controlled switch based on results of the comparisons.

"Matrix Display Having Addressable Display Element's And Methods" Atty. Docket No. CS22497RA

3. The method of Claim 2, controlling the logic-controlled switch includes enabling and disabling the logic controlled switch with a charging capacitor.

5

10

15

4. The method of Claim 1,

activating at least some display elements of the display device at a first refresh rate,

activating other display elements of the display device at a second refresh rate, different than the first refresh rate.

5. A method in a display device comprising an $n \times m$ array of addressable display elements, the method comprising:

activating at least some display elements at a first rate; activating other display elements at a second rate, the second refresh rate less than the first refresh rate.

20

6. The method of Claim 5,

activating the display elements with a corresponding logic controlled display element switch when row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

"Matrix Display Having Addressable Display Element's And Methods" Atty. Docket No. CS22497RA

7. The method of Claim 6,

comparing the row address input and the row electrode input, comparing the column address input and the column electrode

input,

activating the display element with the logic controlled display element switch using the results of the comparisons.

10

5

8. The method of Claim 7, enabling and disabling the logic controlled display element switch with a switch enabling charging capacitor gate controlled by the results of the comparisons.

15

9. The method of Claim 5, activating other display elements at the second rate includes not activating the other display elements.

10. A display device comprising:

20

a plurality of display elements arranged in a matrix,
each display element including a display pixel coupled to a
switch,

each display element including an addressable latch having an output coupled to a controlling input of the switch,

"Matrix Display Having Addressable Display Element's And Methods" Atty. Docket No. CS22497RA

5

15

20

the addressable latch having a row address input and a column address input.

11. The device of Claim 10, the addressable latch having a row electrode input and a column electrode input.

12. The device of Claim 10,

the addressable latch of each display element including row address logic and column address logic having corresponding outputs coupled to the output of the addressable latch,

the row address input coupled to the row address logic, the column address input coupled to the column address logic.

13. The device of Claim 10,

the addressable latch of each display element including first and second comparators, the first comparator having the row address input and a row electrode input, the second comparator having the column address input and a column electrode input,

each display element including a logic device having a first input coupled to an output of the corresponding first comparator, the logic

Exp. Mail No. EV203579142US

"Matrix Display Having Addressable Display Element's And Methods" Atty. Docket No. CS22497RA

5

10

15

20

device having a second input coupled to an output of the corresponding second comparator.

14. The device of Claim 13, the logic device is an AND gate, the output of the addressable latch is an output the logic device

15. The device of Claim 13, a pixel capacitor connected parallel with the display pixel, and a switch enabling capacitor coupled to an input of the switch.

16. The device of Claim 10 is a thin-film-transistor display device.

17. A method in a display device comprising an n x m array of addressable display elements, the method comprising:

selectively activating display elements by individually addressing the display elements to be activated;

reducing power consumption by addressing at least some of the display elements at a first frequency and addressing other display elements at a second frequency, 5

10

15

20

the second frequency less than the first frequency.

18. The method of Claim 17,

selectively activating the display elements includes,

applying a row address input and a row electrode input to control logic of the corresponding display element;

applying a column address input and a column electrode input to the control logic of the corresponding display element;

activating the display element with a logic controlled switch when the control logic inputs satisfy a condition.

19. The method of Claim 18,

comparing the row address input and the row electrode input with the control logic,

comparing the column address input and the column electrode input with the control logic,

activating the display element by enabling the logic controlled switch using the results of the comparisons.

20. The method of Claim 19, enabling and disabling the logic controlled switch with a switch enabling capacitor controlled by the control logic.

5